What is claimed is:

1. A method of forming a silicon oxide layer in a semiconductor manufacturing process, comprising:

forming a planar spin on glass (SOG) layer by coating an SOG composition onto a semiconductor substrate having a stepped portion formed thereon;

pre-baking the substrate at a temperature of from about 100 to about 500°C for about 1 to about 10 minutes;

maintaining a loading temperature of a furnace into which the substrate will be loaded at about 500°C or less;

loading the substrate into the furnace; and

main-baking the substrate at a temperature of from about 500 to about 1200°C for about 10 to about 120 minutes to form a silicon oxide layer on the substrate.

2. The method as claimed in claim 1, further comprising implementing an edge bead removal after forming the SOG layer.

3. The method as claimed in claim 2, further comprising implementing a chemical mechanical polishing (CMP) process after forming the silicon oxide layer.

4. The method as claimed in claim 1, wherein the substrate is pre-baked for about 4 to about 6 minutes at a temperature of from about 130 to about 230°C.

5. The method as claimed in claim 1, wherein the substrate is pre-baked under an atmosphere of air, an oxygen gas, moisture, a mixture of oxygen and moisture, a nitrogen gas or in a vacuum.

6. The method as claimed in claim 1, wherein the main-baking is implemented for about 30 to about 60 minutes.

7. The method as claimed in claim 1, wherein the substrate is main-baked under an atmosphere of air, an oxygen gas, moisture, a mixture of oxygen and moisture, a nitrogen gas or in a vacuum.

8. The method as claimed in claim 1, further comprising increasing a temperature in the furnace by about 7±3°C/min after loading the substrate into the furnace.

9. The method as claimed in claim 8, wherein the temperature of the furnace is increased under an atmosphere of air, an oxygen gas, moisture, a mixture of oxygen and moisture, a nitrogen gas or in a vacuum.

10. The method as claimed in claim 1, wherein the spin-on glass composition is a polysilazane-based spin-on glass composition.

11. The method as claimed in claim 10, wherein the spin-on glass composition comprises:

from about 20 to about 30% by weight of perhydropolysilazane having a structure of $-(SiH_2NH)_n-$ (in which n represents a positive integer), having an average molecular weight of from about 4,000 to about 8,000, and having a molecular weight dispersion degree of from about 3.0 to about 4.0; and

from about 80 to about 70% by weight of a solvent.

12. The method as claimed in claim 11, wherein the spin-on glass composition has a uniform viscosity of from about 1 to about 10 mPa.s at a shear rate of from about 54 to about 420 (1/s).

13. The method as claimed in claim 11, wherein the spin-on glass composition has a contact angle of no more than about 4° with respect to an underlying layer on which the spin-on glass composition is to be coated.

14. The method as claimed in claim 11, wherein the spin-on glass composition includes at least one compound including an element selected

from the group consisting of boron, fluorine, phosphorous, arsenic, carbon and oxygen as an impurity material.

15. The method as claimed in claim 11, wherein the solvent is xylene or dibutyl ether.

16. The method as claimed in claim 1, wherein a thickness of the silicon oxide layer is from about 4,000 to about 6,500 Å.

17. The method as claimed in claim 1, wherein the stepped portion is formed by at least two conductive patterns.

18. The method as claimed in claim 17, wherein a distance between the conductive patterns is in a range of from about 0.04 about 1 μm.

19. The method as claimed in claim 17, wherein the two conductive patterns are gate electrodes or metal wiring patterns of a semiconductor device.

20. The method as claimed in claim 1, wherein an aspect ratio of the stepped portion is in a range of from about 5:1 to about 10:1.

21. The method as claimed in claim 1, wherein the stepped portion includes a closely stepped portion of which an aspect ratio is from about 5:1 to about 10:1 and a global stepped portion of which an aspect ratio is no more than about 1:1.

22. The method as claimed in claim 1, further comprising forming a silicon nitride layer having a thickness of from about 200 to about 600 Å before coating the spin-on glass composition.

23. A method of forming a silicon oxide layer in a semiconductor manufacturing process, comprising:

forming a planar SOG layer onto a semiconductor substrate having a stepped portion formed thereon by coating an SOG composition comprising from about 20 to about 30% by weight of perhydropolysilazane having a structure of $-(SiH_2NH)_n-$ (in which n represents a positive integer), having a weight average molecular weight of from about 4,000 to about 8,000, and having a molecular weight dispersion degree of from about 3.0 to about 4.0, and from about 80 to about 70% by weight of a solvent;

pre-baking the substrate at a temperature of from about 130 to about 230°C for about 4 to about 6 minutes;

maintaining a loading temperature of a furnace into which the substrate will be loaded at about 500°C or less;

loading the substrate into the furnace and increasing the temperature of the furnace by about 7±3°C/min; and

main-baking the substrate at a temperature of from about 500 to about 1200°C for about 30 to 60 minutes to form a silicon oxide layer on the substrate.

24. The method as claimed in claim 23, further comprising implementing an edge bead removal after forming the SOG layer, and implementing a CMP process after forming the silicon oxide layer.

25. The method as claimed in claim 23, wherein an aspect ratio of the stepped portion is in a range of from about 5:1 to about 10:1.